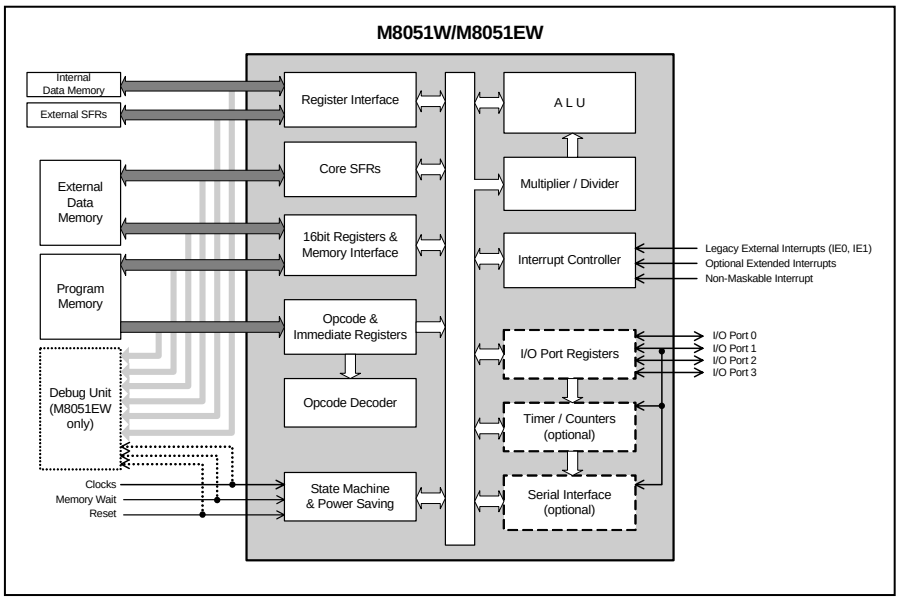
M8051EW

Fast 8-bit Microcontroller with On-Chip Debug

Soft Core (RTL IP)

D A T A S H E E T



M8051EW Block Schematic

Overview

The M8051EW offers a complete, high performance 8051 core and development kit, based around Mentor Graphics's highly successful M8051W implementation of this popular 8-bit microcontroller. While the standard part is designed around a 12-clock machine cycle, both the M8051W and the M8051EW use a two-clock machine cycle to facilitate particularly fast and/or low power embedded solutions whilst retaining functional compatibility with the industry standard part.

It also features support for both up to 1 Mbyte of Program memory and up to 1 Mbyte of external Data Memory. The IP is supported by many 3rd-party C compilers and assemblers. For example, Mentor Graphics uses the C51 compiler from Keil Software for internal development and testing.

The M8051EW also features a Debug Mode in which it can be driven in single-step fashion through a dedicated Debug interface. This aspect of the M8051EW is intended for use with First Silicon Solutions (FS2)'s In-Target System Analyzer for the M8051EW to provide a range of debugging features from basic stop/start or single-step execution and breakpoint support to reconstruction of execution history and capture of data memory, program memory and SFR accesses.

The M8051EW can be configured to suit a wide range of user requirements. For example, it can be configured to work with either synchronous or asynchronous memory; it can have separate Program and External Data Memory interfaces or a single multiplexed interface; and it can offer either one, two, four or eight data pointers and up to 24 maskable interrupts at two or four levels of interrupt priority.

Wait state support is provided for slow memory devices.

Major product features:

- Two clocks per machine cycle architecture
- JTAG Interface and software for debug
- Up to 1 Mbyte of external Data Memory, accessible by a choice of interfaces
- Up to 256 bytes of Internal Data Memory
- Up to 1 Mbyte of RAM or ROM Program Memory, accessible by a choice of interfaces
- Support for synchronous and asynchronous Program, External Data & Internal Data Memory
- Wait states support for slow Program and External Data Memory
- Software compatible with Intel 8051, 8031, 87C51 and 8052 equivalents
- 2 or 3 16-bit timer/counters (optional)
- Full-duplex serial port (optional)
- Intel-compatible I/O ports
- Max 25 source, 2 or 4-level interrupt controller; choice of handling scheme
- Option of 1, 2, 4 or 8 data pointers
- Support for user-defined SFRs
- Separate demultiplexed memory interface ports
- Fully synthesizable
- Scan test ready

Deliverables:

- Verilog & VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL testbenches
- Reference technology netlist
- Product Specification & User Guide

Related Products:

- M8051W Fast 8-bit Microcontroller

Mentor Graphics

Design Features

TWO CLOCK MACHINE CYCLES: This allows the device either to run at up to six times the speed at the same power consumption or to use one sixth of the power when running at the standard speed. All instructions have zero-wait-state execution times that are exactly $^1/_6$ those of the standard part.

DEBUG SUPPORT: The M8051EW offers a Debug Mode together with a set of dedicated Debug signals which may be used by external debug hardware to provide start/stop program execution in response to both hardware and software triggers, single step operation and program execution tracing.

It is envisaged that these facilities will be used in conjunction with First Silicon Solutions (FS2)'s In-Target System Analyzer for the M8051EW.

INTERRUPT STRUCTURE: The M8051EW supports between 5 and 24 maskable interrupt sources under two handling schemes ('Standard' and 'Grouped Priority') at either 2 or 4 levels of priority – all depending on selections made in the M8051EW configuration file when the design is compiled. The Vector locations of these interrupts are identical to those used by the Keil Software C51 compiler, allowing their use in conjunction with this compiler. The design also includes a Non-Maskable Interrupt which takes priority over all other interrupts.

POWER-SAVING MODES: The M8051EW has two power-saving modes: Power Down mode and Idle mode. In Power Down mode, the clock to the entire M8051EW is stopped. In Idle mode, the clock to the CPU is stopped but the timer/counters and the serial port are still active.

The peripheral clock driving the interrupt controller, the timer/counters and the serial interface is half the frequency of the core (CPU) clock i.e. once per machine cycle, giving further power savings over the standard 12-state part.

SERIAL PORT AND TIMER/COUNTERS: The inclusion of a serial port and timer/counters within the M8051EW simplifies the system design required for a range of possible applications. The serial port is full duplex. It is also receive buffered. If, however, either the serial port or any of the timer/counters are not required for a particular application, these items can readily be omitted at compile time.

DATA & PROGRAM MEMORY: The M8051EW can address up to 1 Mbyte of Program RAM or ROM and up to 256 bytes of internal Data Memory (implemented as dual-port RAM in the target technology).

The M8051EW can also address up to 1 Mbyte of external Data RAM. This external Data memory is accessed through either the program memory interface or a dedicated memory bus rather than via the I/O ports. The 32 port pins are therefore used exclusively for peripheral I/O.

Slow external data and program memory may assert a memory wait signal to stall CPU activity, whilst leaving peripheral functions unaffected. Each program and data memory interface may be configured to support either asynchronous or synchronous memory devices.

Note: Two methods are offered for addressing memory above the standard 64Kbytes. One is a built-in 'Memory Extension' scheme. The alternative approach is to use standard code banking techniques. Many standard 8051 assemblers and C compilers (including the Keil compiler recommended above) support code banking.

USER-DEFINED SPECIAL FUNCTION REGISTERS: Depending on the core configuration, up to 119 'External' special function registers (ESFRs) may be added to the M8051EW core, up of 11 which may be bit-addressable. ESFRs are memory mapped into Direct Memory between addresses 80 hex and FF hex in the same manner as core SFRs and may occupy most addresses not occupied by a core SFR.

Reference Technology Gate Count: Intel-compatible implementation 8160; max. 19230 with OCI (excluding ROM and RAM)

THE M8051 FAMILY OF MICROCONTROLLER CORES

Design	Clocks/ machine cycle	Program Space	Ext. Data Space	Int. Data Bytes	Multiplexed Prog + Data Memory	Synch. Memory Support	Memory Wait States Support	Program Memory Write Instr.	Interrupt Sources	Non-Maskable Interrupt	Interrupt Levels	Data Pointers	I/O Ports	Timer Counters	UART	Memory Banking	Interface for Extra SFRs	JTAG I/F + Debug s/w
M8051	12	0-64K	0-64K	0-256	✓				5		2	1	4	2	1	✓	✓	
M8052	12	0-64K	0-64K	0-256	✓				6		2	1	4	3	1	✓	✓	
M8051W	2	0-1M	0-1M	0-256	✓	✓	✓	✓	5 – 24	✓	2/4	1/2/4/8	0/4	0/2/3	0/1	✓	✓	
M8051EW	2	0-1M	0-1M	0-256	✓	✓	✓	✓	5 – 24	✓	2/4	1/2/4/8	0/4	0/2/3	0/1	✓	✓	✓

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05/05 PD-40105.004-FO